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EXAMINER	
WILSON, SCOTT R	

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2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/745,114	Applicant(s) YANG, SAM
	Examiner Scott R. Wilson	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32,73-106 and 110-127* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,12,28,29,73,81,82,87-89,93-95,99-101,105,110,118,126 and 127* is/are rejected.

7)☒ Claim(s) *2-11,13-27,30-32,74-80,83-86,90-92,96-98,102-104,106,111-117 and 119-125* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *14*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 126 and 127 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al.. Tanaka et al., Figure 7B, discloses a capacitor comprising a first electrode (24)(col. 10, line 42), a second electrode (22A)(col. 10, line 54), a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode.

As to claim 126, Tanaka et al., Figure 7B, discloses the dielectric layer (23) directly adjoins the first electrode (24), and the metal oxide buffer layer (22B) directly adjoins the dielectric layer (23) and the second electrode (22A).

As to claim 127, Tanaka et al., Figure 7B, discloses that the dielectric layer (23) comprises a single layer.

Claim 12 is rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al.. Tanaka et al., Figure 7B, discloses a vertical capacitor comprising a bottom electrode (22A)(col. 10, line 54), a top electrode (24)(col. 10, line 42) positioned above the bottom electrode, a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode.

Claims 28 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al.. As to claim 28, Tanaka et al., Figure 7B, discloses a vertical capacitor comprising a bottom electrode (22A)(col. 10, line 54), a top electrode (24)(col. 10, line 42) positioned above the bottom electrode, a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. Tanaka et al. also discloses (col. 4, lines 7-8) the metal oxide formed by annealing, therefore being within the scope of an annealed metal oxide.

As to claim 29, Tanaka et al. discloses that the lower electrode (22A) is formed from ruthenium (col. 9, Table 3) and that the metal oxide layer (22B) is formed from ruthenium oxide (col. 9, line 39).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ino in view of Tanaka et al.. Ino, Figure 1, discloses a semiconductor die comprising an integrated circuit supported by a substrate (1) and having a plurality (col. 1, line 20-21) of integrated circuit devices wherein at least one of the plurality of integrated circuit devices comprises a capacitor (10), (11) and (12). Ino does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first

electrode and the second electrode. Tanaka et al., Figure 7B, discloses a capacitor comprising a first electrode (22A)(col. 10, line 54), a second electrode (24)(col. 10, line 42), a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the die of Ino with the capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Ino to obtain the invention as specified in claim 73.

Claims 81 and 82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Tanaka et al.. As to claim 81, Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Tanaka et al., Figure 7B, discloses a capacitor comprising a first electrode (22A)(col. 10, line 54), a second electrode (24)(col. 10, line 42), a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Yoneda to obtain the invention as specified in claim 81.

As to claim 82, Tanaka et al. discloses that the lower electrode (22A) is formed from ruthenium (col. 9, Table 3) and that the metal oxide layer (22B) is formed from ruthenium oxide (col. 9, line 39).

Claim 87 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Tanaka et al.. Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Tanaka et al., Figure 7B, discloses a vertical capacitor comprising a bottom electrode (22A)(col. 10, line 54), a top electrode (24)(col. 10, line 42) positioned above the bottom electrode, a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. Tanaka et al. also discloses (col. 4, lines 7-8) the metal oxide formed by annealing, therefore being within the scope of an annealed metal oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Yoneda to obtain the invention as specified in claim 87.

Claims 88 and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. in view of Tanaka et al.. As to claim 88, Chu et al., Figure 2, discloses a memory module comprising a support (10), a plurality of leads extending from the support (8), a command link (19) coupled to at least one of the plurality of leads, a plurality of data links (Fig. 3, element 54) wherein each data link is coupled to at least one of the plurality of leads and memories (20), (22), (40) and (42) contained on the support and coupled to the command link, wherein the memories comprise an array of memory cells with

capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Chu et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Tanaka et al., Figure 7B, discloses a capacitor comprising a first electrode (22A)(col. 10, line 54), a second electrode (24)(col. 10, line 42), a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Chu et al. with the capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Chu et al. to obtain the invention as specified in claim 88.

As to claim 89, Tanaka et al. discloses that the lower electrode (22A) is formed from ruthenium (col. 9, Table 3) and that the metal oxide layer (22B) is formed from ruthenium oxide (col. 9, line 39).

Claim 93 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. in view of Tanaka et al.. Chu et al., Figure 2, discloses a memory module comprising a support (10), a plurality of leads extending from the support (8), a command link (19) coupled to at least one of the plurality of leads, a plurality of data links (Fig. 3, element 54) wherein each data link is coupled to at least one of the plurality of leads and memories (20), (22), (40) and (42) contained on the support and coupled to the command link, wherein the memories comprise an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Chu et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide

buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Tanaka et al., Figure 7B, discloses a vertical capacitor comprising a bottom electrode (22A)(col. 10, line 54), a top electrode (24)(col. 10, line 42) positioned above the bottom electrode, a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. Tanaka et al. also discloses (col. 4, lines 7-8) the metal oxide formed by annealing, therefore being within the scope of an annealed metal oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Chu et al. with the capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Chu et al. to obtain the invention as specified in claim 93.

Claims 94 and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Tanaka et al.. As to claim 94, Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Tanaka et al., Figure 7B, discloses a capacitor comprising a first electrode (22A)(col. 10, line 54), a second electrode (24)(col. 10, line 42), a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the

capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Le et al. to obtain the invention as specified in claim 94.

As to claim 95, Tanaka et al. discloses that the lower electrode (22A) is formed from ruthenium (col. 9, Table 3) and that the metal oxide layer (22B) is formed from ruthenium oxide (col. 9, line 39).

Claim 99 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Tanaka et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Tanaka et al., Figure 7B, discloses a vertical capacitor comprising a bottom electrode (22A)(col. 10, line 54), a top electrode (24)(col. 10, line 42) positioned above the bottom electrode, a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. Tanaka et al. also discloses (col. 4, lines 7-8) the metal oxide formed by annealing, therefore being within the scope of an annealed metal oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Le et al. to obtain the invention as specified in claim 99.

Claims 100 and 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Tanaka et al.. As to claim 100, Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Tanaka et al., Figure 7B, discloses a capacitor comprising a first electrode (22A)(col. 10, line 54), a second electrode (24)(col. 10, line 42), a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Le et al. to obtain the invention as specified in claim 100.

As to claim 101, Tanaka et al. discloses that the lower electrode (22A) is formed from ruthenium (col. 9, Table 3) and that the metal oxide layer (22B) is formed from ruthenium oxide (col. 9, line 39).

Claim 105 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Tanaka et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells

with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Tanaka et al., Figure 7B, discloses a vertical capacitor comprising a bottom electrode (22A)(col. 10, line 54), a top electrode (24)(col. 10, line 42) positioned above the bottom electrode, a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. Tanaka et al. also discloses (col. 4, lines 7-8) the metal oxide formed by annealing, therefore being within the scope of an annealed metal oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Le et al. to obtain the invention as specified in claim 105.

Claim 110 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Tanaka et al.. As to claim 110, Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda further discloses in Figure 1, a memory cell comprising a capacitor (5) and an access device (1b), embodied as a wordline. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric

layer and an electrode selected from the group consisting of the first electrode and the second electrode. Tanaka et al., Figure 7B, discloses a capacitor comprising a first electrode (22A)(col. 10, line 54), a second electrode (24)(col. 10, line 42), a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Le et al. to obtain the invention as specified in claim 110.

Claim 118 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Tanaka et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. further discloses that the processor is electrically connected to a memory cell via the data link. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Tanaka et al., Figure 7B, discloses a capacitor comprising a first electrode (22A)(col. 10, line 54), a second electrode (24)(col. 10, line 42), a single compound dielectric layer (23)(col. 10, lines 62-64) interposed between the first electrode and the second electrode and a metal oxide buffer layer (22B)(col. 10, line 46) intermediate the dielectric layer and the first electrode. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the

memory system of Le et al. with the capacitor of Tanaka et al.. The motivation for doing so would have been to form an electrode, a dielectric capacitor of which is not degraded by long-duration exposure to a high-temperature environment (Tanaka et al., col. 2, lines 31-34). Therefore, it would have been obvious to combine Tanaka et al. with Le et al. to obtain the invention as specified in claim 118.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claim 1 is provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of copending Application No. 10/215462. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claim 12 is provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 12 of copending Application No. 10/215462. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claim 28 is provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 28 of copending Application No. 10/215462. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Allowable Subject Matter

Claims 2-11, 13-27, 30-32, 74-80, 83-86, 90-92, 96-98, 102-104, 106, 111-117 and 119-125 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 703-308-6557. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

srw
December 14, 2003